FPGA Implementation of a Self Healing Strategy for Interconnect Faults in Digital Measurement Circuits

S. Meyyappan, V. Alamelumangai

Abstract

The paper attempts to evolve a design mechanism with a view to address the predictive occurrence of interconnect faults in digital measurements acquired through combinational circuits. The system inherits a facility to analyse the flow of signal at all intermediate levels to ensure the comprehensive fault tolerant status. The procedure avails the role of a standard decoder circuit to explore the strength of the methodology and establish its feasibility in a FPGA environment. The generation of test patterns skim the nuances of the existing schemes to arrive at the timing diagrams to suit both stuck at zero and stuck at one faults. The methodology attaches a self healing nature and ventures to carry through the signal in accordance with the attributes of specific application requirements. The FPGA based experimental results obtained validate the simulation exercises in the Modelsim platform and reopen a paradigm shift in the scope of digital circuits.

Keywords: Fault tolerance, FPGA, Self healing, Stuck at faults, VHDL.

1 Introduction

The measurement of variables pronounces the role of a digital arrangement to exploit the innate merits of the binary system and make use of the speed and flexibility that revolves around it. A reliable hardware performance augurs a significant requirement to ensure a sense of authentication in a digital measurement system. However improper functioning of the logic circuits in a digital system manifests itself as either permanent or transient deviations of logic variables from the values specified in design. While the permanent faults arise due to physical changes in the components of a logic circuit, the transient faults creep in owing to temporary changes in the properties of logic circuits. The faults differ in their extent in the sense a local fault affects only one logic circuit and a distributed fault carries its influence in several logic circuits of the same system.

Digital fragility can be reduced by designing a digital system that enforces the state transition logic to reach the unused states and trigger a reset sequence to arrive at an appropriate error recovery routine. The predominant nature of digital systems emphasizes the precise operating states when the underlying bits are reliable enough so that errors cannot influence their performance.

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However there arises the probability of unforeseen errors that may creep in the connecting wires and the origin of extraneous noise signals along with the usual path sensitization defects can prevent the functional operation and lead to undefined states. Thus testing assumes significance to guarantee fault-free devices and improve the quality of service at the various stages of either a manufacturing system or in the control of a process and similar other activities.

The basic concepts that include the need for fault tolerant systems and techniques of fault tolerance have been outlined in [4]. The theory of redundancy programmability, reliability modelling and prediction and approaches to the problem of tolerating design faults have been explained in [10].

The existing scheme for the design of self-checking circuits based on duplication has been presented in [3]. The problem of synthesizing self checking two level combinational circuits has been addressed using three concurrent error detection schemes in [12] and [14]. A cost effective non intrusive technique of partially checking combinational circuit has been developed in [2]. A heuristic procedure has been described to find the optimal sum of product expression and to evaluate the effectiveness of the methodology. A functional cell in the architecture of FPGA has been used to implement logic functions and to route signals to other cells in [9]. The fault tolerant address generator has been programmed using a look up table approach to correct single error in the incoming data to the functional cell. A fault detection strategy has been developed for a combinational circuit with basic boolean logic in [11]. The probability of the occurrence of stuck at zero or stuck at one in parallel bus lines has been analysed and fault tolerant design solved in [13].

However in view of the sophisticated nature of the measurement variables it creates a need to explore methods that can efficiently predict the occurrence of faults and attach a sense of security to the transmission of data. The primary goal of the work is to address stuck at faults through deductive techniques. An attempt is made to foresee their occurrence and concatenate measures to prevent the logical combinations of such undesirable measurement inputs. The paper organizes itself under four headings that include the design methodology of the proposed scheme, simulation responses, hardware results and finally conclusion.

2 Design Methodology

A fault model is an engineering prediction of something that may go wrong in the operation of a piece of equipment. The focus spreads to anticipate the consequences of a particular fault and spring up patterns to ascribe the fault tolerant feature as part of the design.

The single stuck-at-fault categorises a frequent appearance where in one of the signal lines in the circuit assumes to be stuck at a fixed logic value, regardless of the inputs. Hence in a circuit with n signal lines the potential possibility extends to $2n$ stuck-at faults defined on the circuit. The stuck-at fault bears logical and permanent fault characteristics in contrast to intermittent faults which occur at random states.

The proposed methodology evolves a simple procedure to heal stuck at faults at interconnect levels of the system in the sense that it reacts to the occurrence of a fault at one of the intermediate signals and brings out a fault free output. It engraves the function of as many decoders together with a similar reference entity to cleave the algorithm and arrive at the design prodigy.

The block diagram shown in Fig. 1 explains the stages involved in the healing mechanism and primarily comprises of an appropriate number of ex-or gates, priority encoders and multiplexers to rig out the correct output. The circuit under test is triplicated, of which one coerces to function as the reference module to aid in the process of detection. The similar outputs and its copies constitute the inputs to the ex-or gates and compared with the similar outputs of the reference circuit. The similar outputs of the ex-or gates travel to the priority encoders to generate the select lines for the multiplexers and there from restore the true output. The steps lined below outline the procedure encircling the algorithm.

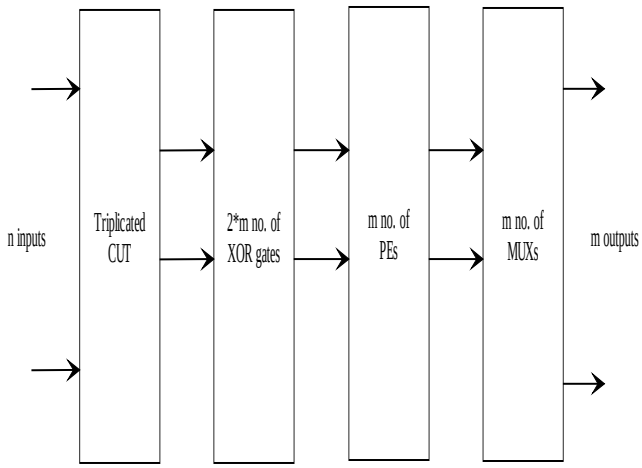

Fig. 1 Block diagram of the proposed self healing system

3 Algorithm

1. Assign values to the primary inputs
2. Simulate and record the primary outputs obtained.
3. Choose the intermediate signals of the system randomly
4. Inject fault on the chosen signals
5. Perform simulation again and record the output values
6. Validate the performance of the system by comparing the values obtained in step (3) and (5)

4 Simulation

The development in the field of VLSI though reduced chip dimensions, carries with it a detrimental effect on the reliability of a system in view of the high degree of errors that range over a varied class [7] and [8]. An immediate way out to cope up with faults in digital systems necessitates to incorporate fault tolerance in the system [5]. The primary goal of fault tolerance assembles to restore the normal operation of the system even in the presence of faults [6].

The circuit under test comprises of a three level combinatorial circuit in the form of a decoder. The digital signals that correspond to the measurements made enter the two decoders and a reference unit from where it reaches parallelly to the top and bottom set of ex- or gates. The design carves out the introduction of specific faults and edges out measures to replace the faulty signal and allow its passage to the group of priority encoders where from it generates the enable input for the multiplexer. The output constitutes the true fault free digital parameter, a record of which ensures a reliable measurement system for a wide variety of users.

The facility ensembles the role of the available circuits and realizes their function through VHDL description. The scheme examines the self healing ability of the proposed methodology using Modelsim (version: 10.2b) based simulation. The first two clock cycles in Fig. 2 and the first four clock cycles in Fig. 3 bring to light the fault free operating status of the system.

The procedure be-hives to offset the toggle type faults created on the decoder output lines in the third and fourth, fifth and sixth clock cycles instantaneously as seen from Fig. 2. The Fig. 3 relates to similar events in the outputs of the ex-or gates and priority encoders in the next four clock cycles respectively and reiterates its capability to remain in the fault tolerant mode.

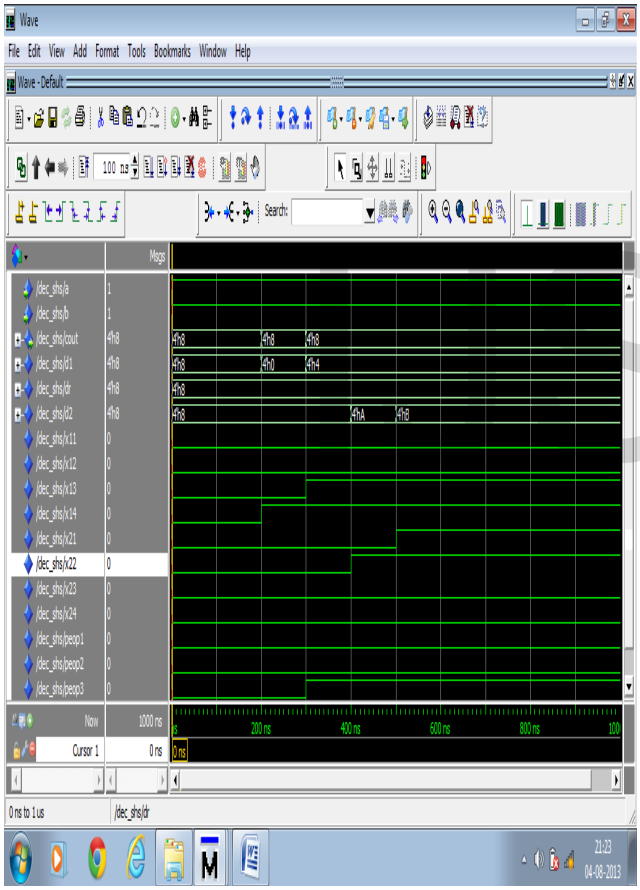

Fig. 2 Output of the self healing system with and without faults in the top entity

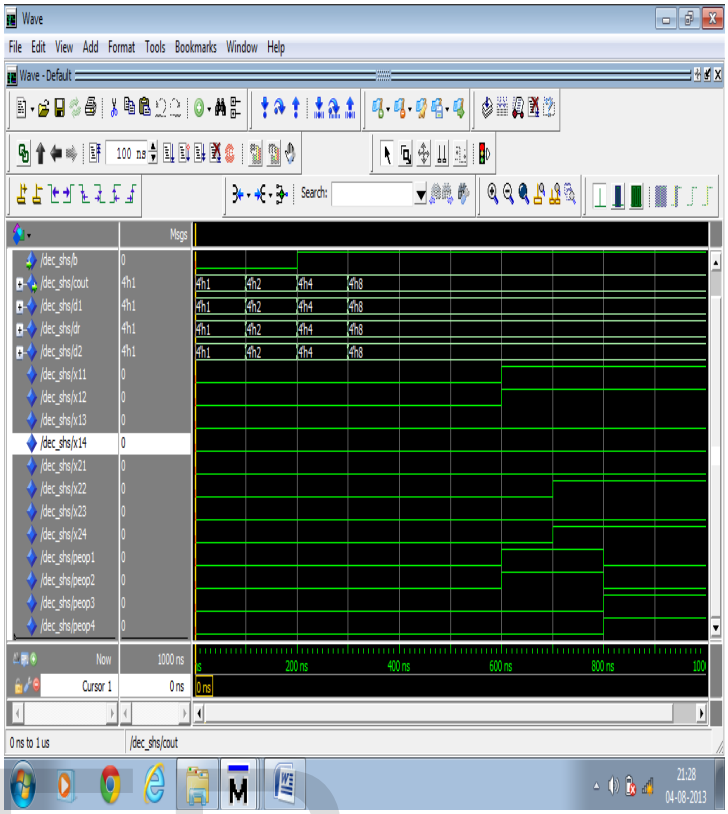

Fig. 3 Output of the self healing system with and without faults at the interconnect level

5 Hardware Implementation

Redundancy realized in a coarse grained level appears to be a general approach to arbitrate on permanent faults in system hardware. Its expensive attributes leave way to exploit the inherent ability of an FPGA to reconfigure itself at a fine grained level and makes it ideal for fault tolerant implementations [1].The Spartan-3E family of Field-Programmable Gate Arrays (FPGAs) augurs to meet the needs of customer based designs and enjoy the inherent inflexibility of conventional ASICs and permits design upgrades to suit specific applications. The snap shot in Fig. 4 shows the experimental setup used to obtain the response of the system under various operating states. The real time implementation of the proposed self healing system using XC3S500E FPGA serves to validate the simulated performance and establish the applicability of the scheme in the real world. The photograph in Fig. 5 illustrates the healing touch for the faults in the decoder lines and the ex-or gates together with the priority encoders through the fact that the LED glow remains the same for all the three cases.

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Fig. 4 Real time experimental set up.

Fig. 5 Validation of the proposed scheme through real time implementation

6 Conclusion

A self healing methodology has been developed to assuage possible occurrences of errors in digital measurement systems. The strategy has been laid to tolerate stuck at faults at the intermediate levels of a digital circuit and correct themselves with fault free outputs. The synthesizable VHDL code has been written to implement the scheme onto XC3S500E FPGA for validating the simulated Modelsim results. The run-time reconfigurable nature of FPGA has been used to detect and cope up with the possible occurrences of faults at the different output lines. The inherent ability of the scheme to correct the interconnect faults in digital circuitry that forms part of a larger periphery acclaims its suitability for practical applications and forge a new dimension for fault tolerance in digital measurements.

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